GSC3e/LPx and GSC3f/LPx

High Performance, Lowest Power, GPS Single Chip

Product Description

The GSC3e/LPx and GSC3f/LPx are the pin-for-pin compatible, lowest power versions of the advanced GSC3e(f)/LP receiver in a single package. The baseband has been ported to 65 nm technology, enabling an additional power reduction of up to 30 percent. In the GSC3e/LPx, the baseband and RF are integrated into the 7 mm x 10 mm x 1.4 mm package. In the GSC3f/LPx, flash memory is included in the package making for an extremely compact design. The GSC3e(f)/LPx includes a powerful GPS DSP integrated with an ARM7TDMI microprocessor and 1 Mb of SRAM. The GSC3e(f)/LPx architecture uses an FFT and Matched Filter that delivers performance equivalent to more than 200,000 correlators. This represents a quantum leap forward in GPS performance.

Architecture Highlights

Next Generation, Lowest Power, GPS Performance

- 200,000+ effective correlators for fast TTFF and high sensitivity acquisitions
- Supports 20-Channel GPS
- High sensitivity for indoor fixes
- Extremely fast TTFFs at low signal levels
- Real-time navigation for location-based services
- Low 100 ms interrupt load on microprocessor for easy IP implementation
- SBAS (WAAS, MSAS, and EGNOS) support

SiRFLoc™ Client AGPS Support

- SiRF patented end-to-end solution
- Multimodes: mobile centric to network centric
- Mutli-standard support: 3GPP, 3GPP2, PDC, iDEN, and TIA-916
- Supports AI3 and F interfaces

GSW3—Modular Software Support

- API compatible with GSW2
- RTOS friendly

Product Highlights

GSC3f/LPx—Digital, RF, and Flash Single Chip

- Digital, RF, and 4 Mb Flash in a single package
- Small 7 mm x 10 mm x 1.4 mm, BGA package
- ARM7TDMI CPU and SRAM to enable user tasks
- Accepts six reference frequencies between 13 MHz and 26 MHz
- Extensive GPS peripherals: 2 UARTs, battery-backed SRAM, and 14 GPIOs

Lowest Power

- Under 60 mW at full power
- 46 mW tracking power
- Push-to-Fix™ reduces power as much as 98%

Built On Proven Experience

- IP integration experience
- Highly developed design tools
- FCC E911 compliance experience

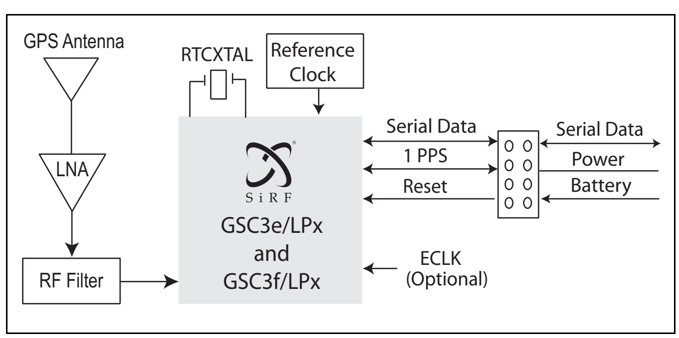


Figure 1. Sample Architecture Diagram

Information Map

SiRFstarIII Architecture Description

SiRFstarIII architecture has the performance required to meet the toughest challenges. SiRFstarIII products can acquire in only seconds even at low signal levels, and can track signal levels as low as -159 dBm. SiRFstarIII architecture supports real-time navigation in urban canyons as well as high sensitivity acquisition needed for attenuated and weak signals.

GSC3e/LPx and GSC3f/LPx Description

The GSC3e(f)/LPx RF section is the most highly integrated lowest-power SiRF RF silicon to date. The RF section integrates an RTC as well as many components that were previously on the board into the silicon while reducing RF die current consumption to 13 mA.

While some A-GPS receivers can experience lengthy acquisition times at low signal levels, SiRFstarIII architecture enables unmatched TTFF at extremely low signal levels. This allows a much richer user experience, which is important because slow or poorly performing applications often fail in the market place.

The GSC3e(f)/LPx can share an RTC and the reference clock is supported by different input frequencies. This means that designs can be simpler and smaller, and batteries can be smaller and last longer.

The small form factor of the GSC3e(f)/LPx in combination with the frequency sharing abilities of the RF section allows for very compact receiver designs. The sensitivity of the GSC3e(f)/LPx can also be used to help overcome non-optimal antennas such as those that are often used in consumer designs.

Functional Description

The GSC3e(f)/LPx is optimized for location applications requiring high performance with low power in a small form factor. The GSC3e(f)/LPx contains a powerful GPS engine built on a low power 65 nm CMOS process with a 1.2 V core. The GSC3e(f)/LPx can run using only 2.85 V power utilizing internal voltage regulators in the digital section. These regulators can be bypassed for lower power consumption if 1.2 V power is available. The internal functions of the digital section are split into two main parts that are defined by the buses that run them. The ARM System Bus (ASB) has all the core CPU components and the SiRF IP bus (SIPB) contains all the GPS and other DSP peripherals. The ARM and DSP share memory for a more cost effective and gate efficient design.

The digital section is described first followed by the RF section.

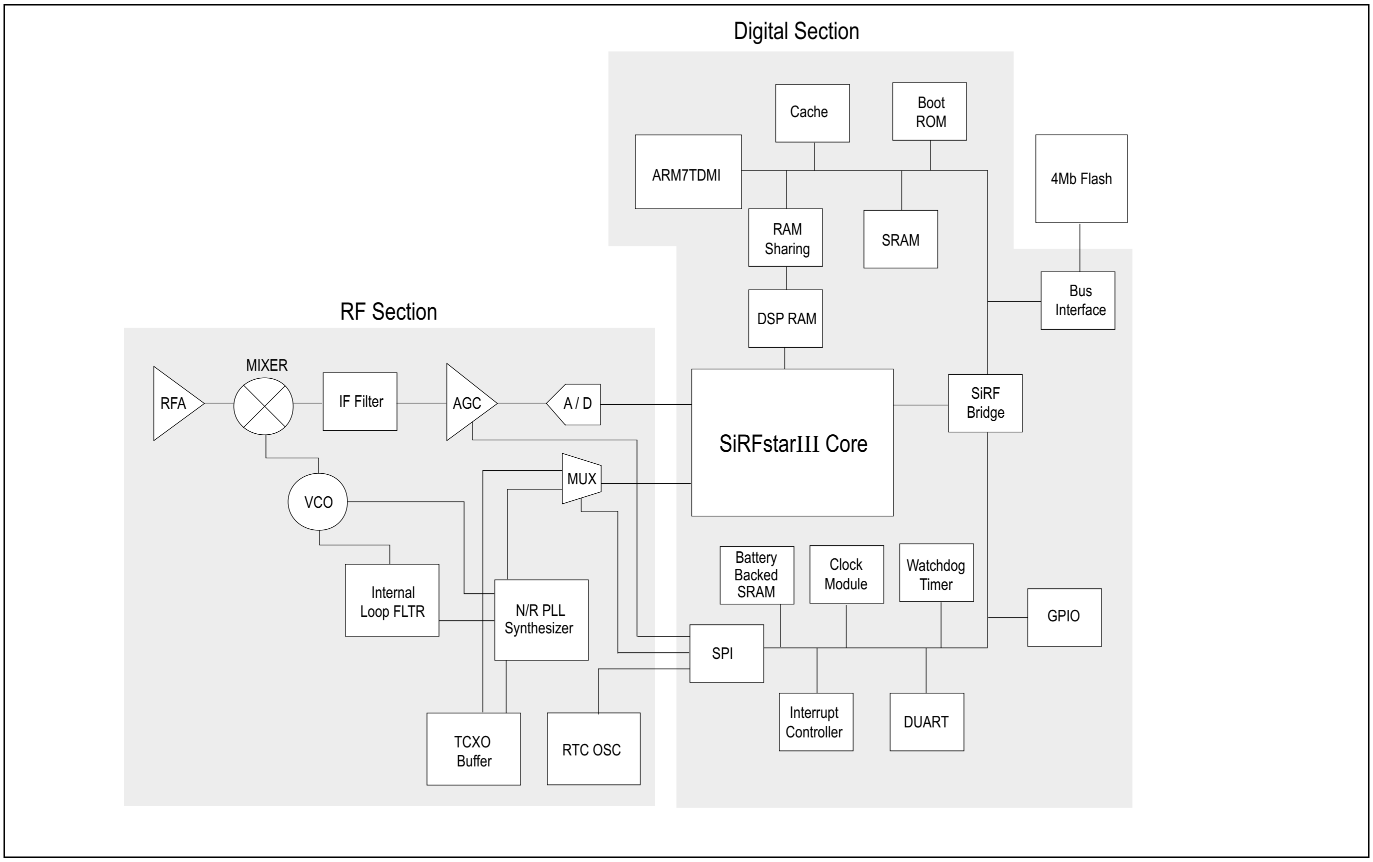


Figure 2. GSC3e(f)/LPx Internal Block Diagram

DIGITAL SECTION DESCRIPTION

SiRFstarIII Core

The SiRFstarIII core is built around a reconfigurable high-output segmented matched filter in conjunction with an FFT processor, which can simultaneously search all 1023 chips of the GPS code over a wide frequency range for fast initial acquisition with large uncertainties. The flexibility of the core allows the core processing engine and memory to be reconfigured to track more than 20 channels using the same hardware. This flexibility makes the SiRFstarIII a highly efficient engine for a wide variety of location applications. The SiRFstarIII core contains a built-in sequencer, which handles all the high-rate interrupts for GPS and SBAS (WAAS, MSAS, EGNOS) tracking and acquisitions. After initialization, the core autonomously handles all time critical and low latency acquisition, tracking and reacquisition tasks of GPS and SBAS. The core provides interrupts, which in turn provides measurement data to the CPU for computation of the navigation solution.

The SiRFstarIII core also provides time and frequency management. This includes the basic clock counters, alarms, edge-aligned ratio counters (EARC) and synchronization blocks used to provide the system time line and to transfer accurate time and frequency into and out of the system. An EARC is an improved (SiRF patented) type of ratio counter used for enhanced frequency accuracy among alternate clocks.

ARM7TDMI

The ARM7TDMI is an ideal core providing high performance and low power consumption. The ARM7TDMI CPU can run at speeds up to 50 MHz and is supported by a wide variety of development tools. Because the SiRFstarIII core eliminates the need for the CPU to service high-rate interrupts, it is easier than ever to use the ARM processing power for user tasks.

The ARM7TDMI includes a JTAG interface, which provides a standard development / debugging interface that connects to a variety of off-the-shelf emulators. This provides single-step, trap and access to all the internal registers of the digital section of the GSC3e(f)/LPx.

Keep-Alive (KA) Section

This group of functions is maintained by a continuous voltage supply from a backup battery.

KA comprises the RTC oscillator (see RF section), RTC counter and comparators (RTC), battery backed SRAM (BB-SRAM) and Finite State Machine (FSM).

Proper power sequencing must be followed to ensure that KA operation is not disrupted by external voltage or current leakage. Refer to Figure 8, “Power Sequencing Diagram,” on page 19.

Battery-Backed SRAM (BB-SRAM)

The GSC3e(f)/LPx contains a small block of battery-backed SRAM, which contains all necessary GPS information for hot starts and a small amount for user configuration variables. BB-SRAM retains critical data from previous operation to enable shorter TTFFs under all startup conditions

RTC Counter and Comparators

The very low-power logic section provides timing for operation of FSM and for self-managed power saving modes such as Adaptive Trickle Power (ATP), Advanced Power management (APM), and Push-To-Fix (PTF). The RTC is critical for operation of hot and warm starts. A large master counter avoids all time ambiguity. Comparators trigger “wake-up” events while in hibernate and are used as event timers during normal operation. The RTC clock frequency is calibrated during operation for optimum hot- and warm-start TTFFs.

Power Control Finite State Machine

The FSM controls power sequencing for all operating modes, including full power mode, and requires a stable RTC clock input.

Inputs to the FSM come from external nSRESET and ON_OFF signals and internal RTC events. nSRESET assertion is allowed and required only when KA section supply voltage is first applied. All other control of power sequences is initiated only by pulses to ON_OFF input, and by serial messages for “soft-off” and power-management configuration.

FSM output controls all internal resets and external control lines nRESET (for JTRST and if needed for external flash memory), nWAKEUP (for control of baseband section voltage supply), RFPWRUP (for control of RF section voltage supply). nWAKEUP and RFPWRUP outputs are required to control proper sequencing of external voltage supplies to RF and baseband in all modes and they enable autonomous self-managed power modes such as ATP, APM, and PTF.

Boot ROM

The Boot ROM contains a small code set that can load a set of user code through UART port A into the SRAM, and execute it. This allows the GSC3e(f)/LPx, for example, to update Flash.

Bus Interface Unit

The Bus Interface Unit (BIU) provides an external 16-bit interface for memory or peripherals supporting half-word transactions. Each chip select addresses a 2-Mbyte address space with an independent start address. The external source for Boot code memory must be selected by $\overline{\text{CS0}}$. The number of wait states for each chip select can be independently set up to a maximum of seven.

Cache

A two-way 8 kB associative instruction/data cache provides a fast access memory for $\overline{\text{CS0}}$ only. GSC3e/LPx will cache only the first 512 KB of external flash memory on CSO while addressing a maximum of 1MB (8Mbits) of external flash memory.

Clock Module

This module generates all internal clocks such as the Signal Processing (SP) Clock and Bus (B) Clock from the Acquisition Clock. The Acquisition Clock is generated by the RF section. The clocks generated by Clock Module run the SiRFstarIII DSP and ARM and control the various power management modes allowing for maximum power savings and system flexibility.

DUART

The GSC3e(f)/LPx contains two full duplex serial ports. One port is normally used for GPS data and receiver control and the second serial port can be used as an alternate communication channel. The transmit and receive side of each port contains a 16-byte deep FIFO with selectable bit rates ranging from 1.2 to 115.2 Kbaud. With special flashing software, maximum baud rate of 921.6 kbps is available.

GPIO Unit

The GSC3e(f)/LPx supports a variety of peripherals through 14 GPIO lines. The GPIO unit centralizes management of all GPIO lines and provides a simple software interface for their control.

FLASH

The GSC3f/LPx integrates 4 Mbits of Flash memory. This eliminates the need for external Flash and significantly simplifies the routing associated with integrating a GPS receiver into a board design. This chip is not available in a pre-flashed version.

Interrupt Controller

The Interrupt Controller manages all internal or external sources of interrupts. These include the SiRFstarIII core, SBAS, DSP, DUART and external user interrupts.

SiRF Bridge Unit

The SiRF Bridge Units (SBU1 and SBU2) provide low power access to peripherals. SBU1 provides access to general purpose ARM peripherals such as the serial port UARTS, RTC, and interrupt controller. SBU2 provides access to the DSP core and its associated memory. The DSP core also uses this bus for internal communications. The ARM is able to perform byte, half-word, and word transactions via the 32-bit peripheral busses.

SRAM

The on-chip SRAM size is 1 Mbit (32k x 32) memory that can be used for instructions or data. In many applications it eliminates the need for external data memory. The SRAM is designed for a combination of low power and high speed, and can support single cycle reads for all bus speeds.

Serial Peripheral Interface

The Serial Peripheral Interface (SPI) port handles communication, such as reference frequency selection, AGC, and power control, between the digital and RF sections. The RF section acts in slave mode and can only be controlled by the digital section using SiRF software. The SPI port consists of SPI_CLK, SPI_DI, SPI_DO, and $\overline{\text{SPI\_CEB}}$ for the RF section, and corresponds to SK, SI, SO, and $\overline{\text{CEB}}$ in the digital section. The SPI port does not support additional SPI devices. It is only used for internal communication between RF and BB.

DSP RAM and RAM Sharing

The GSC3e(f)/LP includes shared RAM which is allocated between ARM and DSP core. This keeps the overall size of the chip down while maximizing the availability of memory.

Factory Testing

The GSC3e(f)/LPx uses a memory built-in self-test called MEMBIST to provide complete coverage of all the memory during chip testing and qualification. This is combined with the SCAN test logic using Automatic Test Pattern Generation (ATPG) at the wafer level to provide functional test coverage. (These functions are not available to customers.)

RF SECTION DESCRIPTION

RF Amplifier (RFA)

The RF section receives the GPS L1 signal via an external antenna and external LNA. The L1 input signal is a Direct Sequence Spread Spectrum (DSSS) signal at 1575.42 MHz with a 1.023 Mbps Bi-Phase Shift Keying (BPSK) modulated code. Because the input signal power at the antenna is nominally -130 dBm (spread over 2 MHz), the desired signal is below the thermal noise floor. With a front-end input compression point of -65 dBm, rejection of large out-of-band signals is possible given filtering in the IF section. The RFA uses a single-ended RF input for ease of use. SiRF run-time firmware provides support for customer production testing of key parameters.

Image-Reject Mixer

The image-reject mixer is a double balanced design, which significantly reduces common mode interference. The Image Reject Mixer block also contains an I-Q phase shift combiner. This circuit properly phase shifts and sums the I and Q outputs internal to the image reject mixer to a single channel and achieves an RF image suppression in excess of 20 dB. By using an image reject mixer, an inexpensive pre-select RF filter may be used. The Mixer and on-chip 1571.424 MHz VCO produce an IF center frequency of 3.996 MHz.

IF Filter

An IF filter is implemented between the Mixer and AGC Amplifier to provide an anti-aliasing function before A/D conversion. In the RF section, the IF filter has been integrated on-chip, thus minimizing the number of external parts on the board. This filter typically provides >20 dB roll-off at the alias frequency (located at F_S-F_{IF}, where F_S is the ADC sample rate), which makes the contribution of C/N_0 degradation due to Nyquist noise folding insignificant. Thus, the combined effects of IF noise aliasing and RF image conversion have a negligible impact to C/N_0 performance.

AGC Amplifier and Control Block

The AGC amplifier provides the additional gain needed to optimally load the signal range of the 2-bit A/D Converter. The AGC IF gain is digitally controlled by an AGC Control block, which loads and registers digital gain setting words from GSC3e(f)/LPx via the four wire SPI interface. The 5-bit AGC Control register allows the SiRFstarIII receiver to compensate for roughly 50 dB variation in system gain for all causes including temperature front-end configuration and process variations.

A/D Converter

The AGC amplifier output drives a 2-bit A/D Converter, which provides sign and magnitude output bits to the Interface block. The combination of 2-bit quantization and oversampling in the SiRFstarIII architecture provides significant improvement in C/N_0 and CW jamming immunity over 1-bit systems.

RTC Oscillator

This circuit is designed to drive a 32.768 kHz crystal. This oscillator is always operational, including during the sleep cycle of the RF section. The main section is specifically designed using a pseudo-inverter topology that provides sufficient gain to start oscillation of the crystal with minimum startup time and minimum current consumption. The crystal is connected between the input and output of this inverter. An internal differential stage followed by a series of inverters is included to convert and drive the oscillation amplitude to CMOS levels. The RTC oscillator circuit also includes start-up circuitry for the bias section to guarantee fast and reliable startup.

Reference Frequency Source

The Reference Clock circuit is designed to be driven by a 13 to 26 MHz TCXO (0.5 ppm temperature coefficient).

Frequency Synthesizer

The RF section GPS down-converter includes an N/R synthesizer that allows the use of a range of reference TCXOs. The synthesizer generates the local oscillator signal for the image reject mixer and also generates the CLKACQ. If the reference clock is selected at 16.369 MHz, the CLKACQ can also be generated from the reference crystal directly (this is the default).

The synthesizer is programmed by software using "N" and "R" words. "N" represents the division ratio of the loop and "R" represents division ratio of the reference signal.

$$[f_{out} / f_{ref}] = N / R$$

N and R inputs are determined by the baseband controller using configuration straps at start-up. The frequencies supported are shown below.

F_{ref} MHz
13
16.369
16.8
19.2
24.5535
26

The local oscillator and sample clock (CLKACQ) are derived from an on-chip PLL synthesizer block. The VCO, dividers, and phase detector are provided in the chip. Use of 16.369 and 24.5535 MHz offers optimal receiver sensitivity.

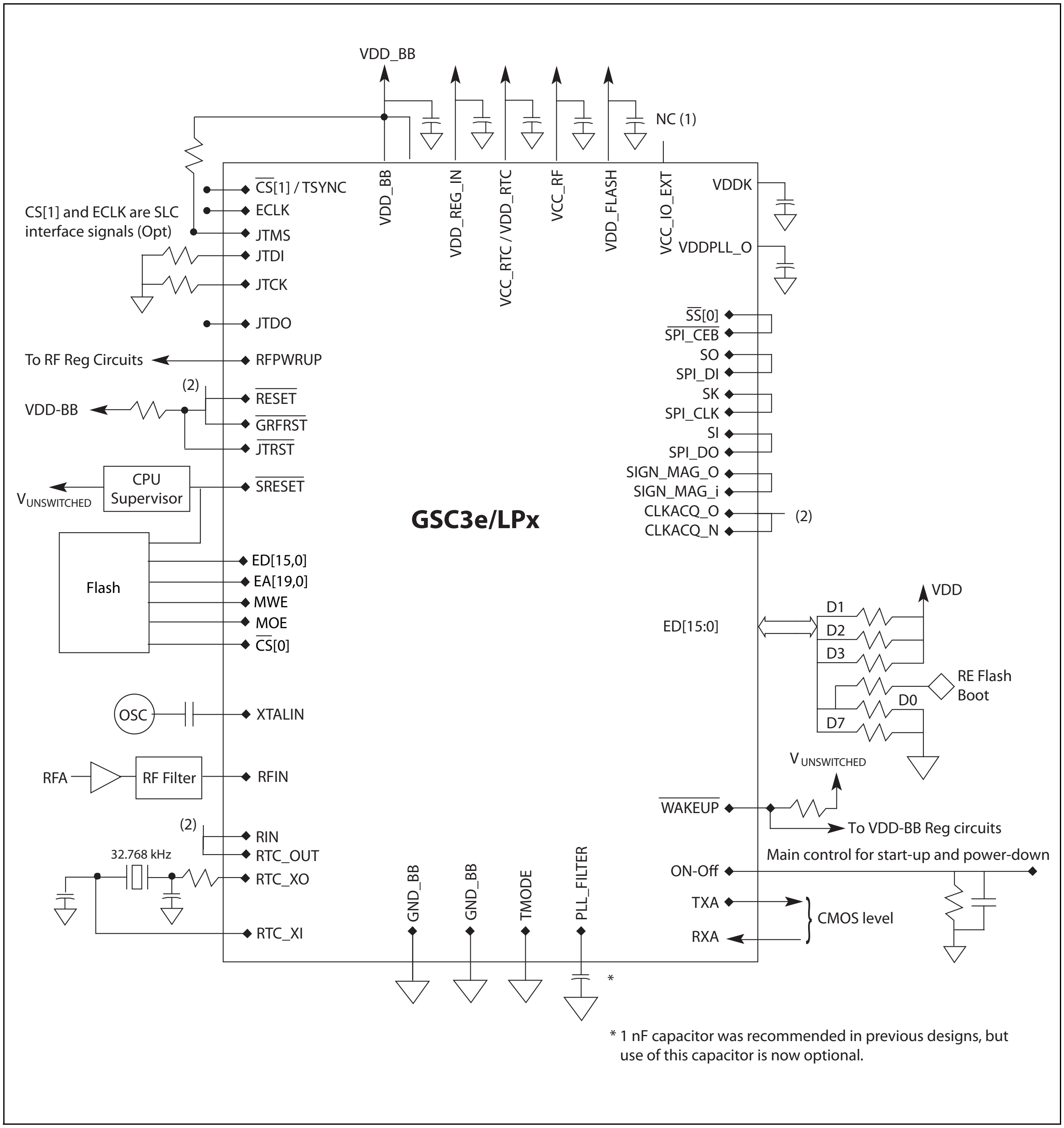
Internal Loop Filter

An internal loop filter is implemented in RF section to reduce pin count and to improve noise immunity on the control node of the VCO. The internal loop filter is automatically adjusted for each input reference frequency to optimize the poles and zeros to achieve optimum loop stability. The loop filter of the RF section synthesizer is an on-chip RC filter.

Clock_Mux

If the system clock is 16.369 MHz, the Clock Mux circuitry allows additional power saving modes by switching off the PLL and using the TCXO reference as the source of the system clock. The selection of the clock is programmed by the digital section through the SPI interface and external boot strap resistors.

Sample Configuration Connection Diagram For GSC3e/LPx



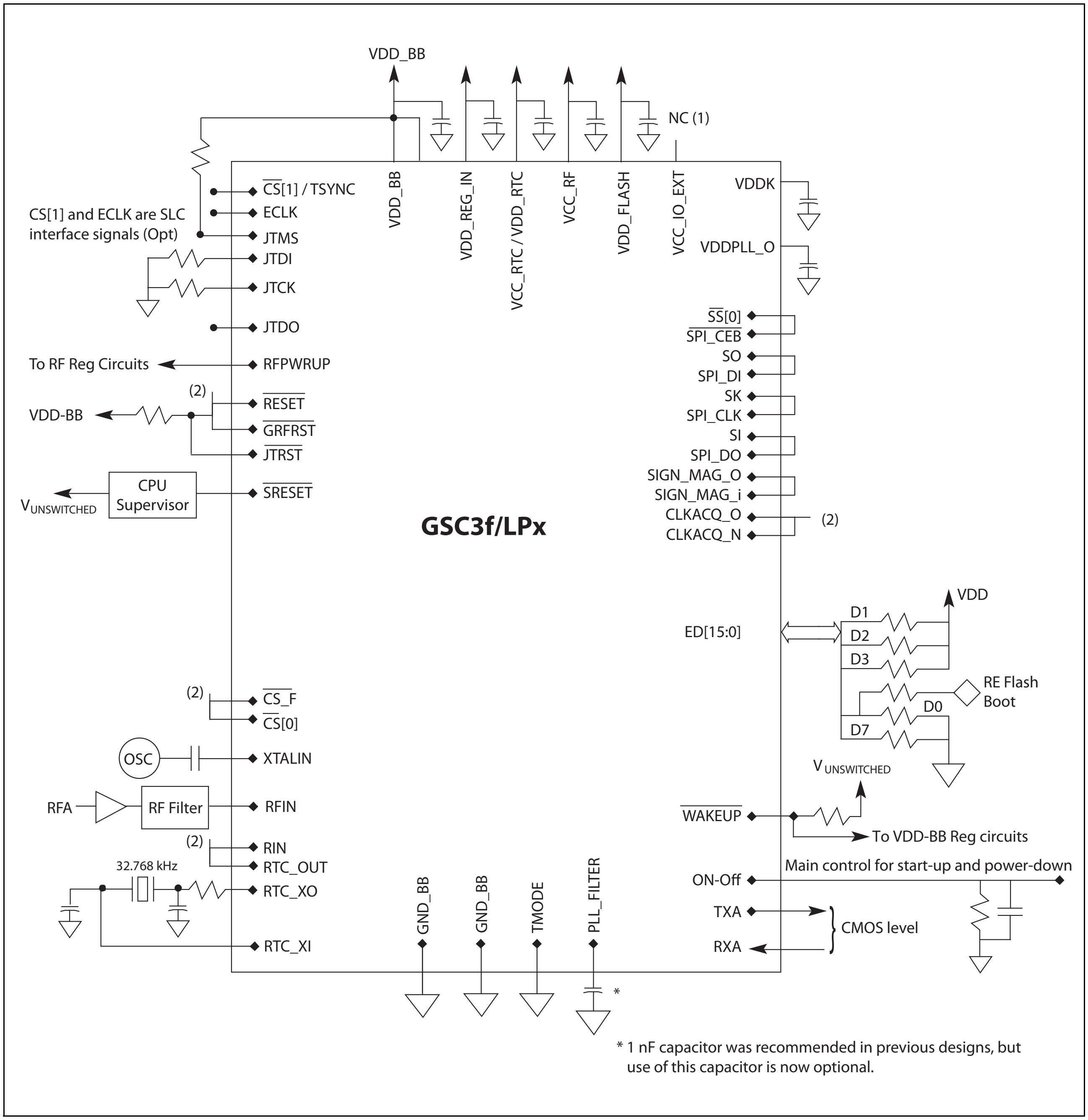
Notes:

(1) VCC-IO-EXT is a no-connect pin. Internal power connections are made and no internal wirebonds connect to PB. This is to enhance the chip ESD performance.

(2) Denotes a very small, short low C test point is desirable.

Figure 3. 7989 Series – 16.369 MHz Configuration

Sample Configuration Connection Diagram For GSC3f/LPx



Notes:

(1) VCC-IO-EXT is a no-connect pin. Internal power connections are made and no internal wirebonds connect to PB. This is to enhance the chip ESD performance.

(2) Denotes a very small, short low C test point is desirable.

Figure 4. 7985 Series – 16.369 MHz Configuration

Ball Configuration

	1	2	3	4	5	6	7	8	9	10
A	GND_BB	GPIO1	CS_F	GPIO[0]	RXA	TXA	ECLK	SCLK	*EA[0]	VDDPLL_O
B	RFPWRUP	MWE	VDD_FLASH	VDD_RTC	EIT[0]	*EA[4]	TXB	Reserved	*EA[1]	VDDK
C	GPIO[14]	ED[1]	*ED[10]	VDD_REG	VDD_PLL	TIMEMARK	RXB	Reserved	*EA[3]	VDDK
D	MOE	*ED[4]	CS[0]	VDD_BB	GND_BB	GND_BB	*EA[2]	*EA[5]	*EA[6]	TMODE
E	GPIO[15]	*ED[9]	*ED[8]	VDD_BB	GND_BB	GND_BB	WAKEUP	*EA[7]	*EA[8]	ROUT
F	GPIO[13]	ED[3]	ED[2]	VDD_BB	GND_BB	GND_BB	VDD_REG	*EA[18]	*EA[19]	RIN
G	ED[0]	*ED[12]	*ED[11]	*ED[14]	*EA[16]	*EA[15]	*EA[13]	*EA[11]	*EA[9]	ON_OFF
H	SS[1]	*ED[5]	*ED[13]	*ED[6]	*EA[17]	PLL_FILTER	*EA[14]	*EA[12]	*EA[10]	RESET
J	JTDI	ED[7]	*ED[15]	CLKACQ_I	SIGN_MAG_I	SI	SK	SO	SS[0]	SRESET
K	JTRST	VDD_BB	AGCPWM	CLKACQ_O	SIGN_MAG _O	SPI_DO	SPI_CLK	SPI_DI	SPI_CEB	RTC_OUT
L	JTMS	VDD_BB	VDD_BB	GND_RF	GND_RF	GND_RF	GND_RF	GND_RF	GND_RF	RTC_XO
M	JTDO	VCC_RF	VCC_RF	VCC_RF	VCC_RF	VCC_RF	VCC_RF	VCC_RF	VCC_RF	VCC_RF
N	JTCK	GND_RF	GND_RF	GND_RF	GND_RF	GND_RF	GND_RF	GND_RF	GND_RF	GND_RF
P	GRFRST	XTAL_IN	XTAL_OUT	TP_IF	GND_RF	RFIN	GND_RF	NC[3]	VCC_RTC	RTC_XI
	1	2	3	4	5	6	7	8	9	10

Notes
1. * = Available for flash pre-loading for customers who use a special flash programmer with GSC3f/LPx compatible socket.
2. Refer to Table 1. for signals that have alternate functions.
3. In GSC3f-7879, this pin was VCC_IO_EXT. To meet the ESD_HBM 2000V, it is internally connected to VCC_RF. No internal wirebonds connect to this ball.

Figure 5. GSC3e/LPx and GSC3f/LPx 140 Pin BGA Ball Configuration Diagram

Table 1. GSC3e(f)/LPx Series Pin Identification

Name	Ball	Name	Ball	Name	Ball	Name	Ball
AGCPWM/GPIO[2]	K3	GND_RF	P5	ED[11]	G3	$\overline{SS}$[0] / GPIO[3]	J9
CLKACQ_I (In)	J4		P7	ED[14]	G4	$\overline{SS}$[1]/ GPIO[4]	H1
CLKACQ_O (Out)	K4	GPIO[0]/LNA EN	A4	EA[16]	G5	TIMEMARK / GPIO[9]	C6
$\overline{CS}$[0]	D3	GPIO[1] / ODO	A2	EA[15]	G6	TMODE	D10
GPIO[13] / $\overline{CTS}$	F1	GPIO[14]/ $\overline{RTS}$	C1	EA[13]	G7	TP_IF	P4
$\overline{CS\_F}$	A3	GPIO[15]/YCLK	E1	EA[11]	G8	TXA	A6
ECLK	A7	$\overline{GRFRST}$	P1	EA[9]	G9	TXB	B7
ED[0]	G1	JTCK	N1	ED[5]	H2	NC	P8
ED[1]	C2	JTDI	J1	ED[13]	H3	VCC_RF	M3
ED[2]	F3	JTDO	M1	ED[6]	H4		M4
ED[3]	F2	JTMS	L1	EA[17]	H5		M5
ED[7]	J2	$\overline{JTRST}$	K1	EA[14]	H7		M6
EIT[0] / GPIO[10]	B5	$\overline{MOE}$	D1	EA[12]	H8		M7
GND_BB	A1	$\overline{MWE}$	B2	EA[10]	H9		M8
	D5	ON_OFF	G10	ED[15]	J3		M9
	D6	PLL_FILTER	H6	$\overline{RESET}$	H10		M10
	E5	EA[0]	A9	RFIN	P6	VCC_RF	M2
	E6	EA[4]	B6	RFPWRUP	B1	VCC_RTC	P9
	F5	Reserved	B8	RIN	F10	VDD_BB	D4
	F6	EA[1]	B9	RTC_OUT	K10		E4
GND_RF	L4	ED[10]	C3	RTC_XI	P10		F4
	L5	Reserved	C8	RTC_XO	L10		K2
	L6	EA[3]	C9	RXA	A5		L2
	L7	ED[4]	D2	RXB	C7		L3
	L8	EA[2]	D7	SCLK	A8	VDD_FLASH	B3
	L9	EA[5]	D8	SI	J6	VDD_PLL	C5
	N2	EA[6]	D9	SIGN_MAG_I (In)	J5	VDD_REG	C4
	N3	ED[9]	E2	SIGN_MAG_O (Out)	K5		F7
	N4	ED[8]	E3	SK	J7	VDD_RTC	B4
	N5	EA[7]	E8	SO	J8	VDDK	B10
	N6	EA[8]	E9	$\overline{SPI\_CEB}$	K9		C10
	N7	Reserved	E10	SPI_CLK	K7	VDDPLL_O	A10
	N8	EA[18]	F8	SPI_DI	K8	$\overline{WAKEUP}$	E7
	N9	EA[19]	F9	SPI_DO	K6	XTAL_IN	P2
	N10	ED[12]	G2	$\overline{SRESET}$	J10	XTAL_OUT	P3

Table 2. GSC3e(f)/LPx Signal Description

Signals	Type	Description
Address and Data Pins - CPU Interface		
CS[0] [1, 3]	O	Flash memory chip select.
CS_F [1]	In	Internal Flash Chip Select
ECLK [2]	In	External CMOS clock source.
EA[19:0]	O	External address bus.
ED[15:0]	I/O	External data bus. ED[3:0] are used for strap options.
ED[0] [4]	I/O	Read on power-up to determine start address: 1 = internal ROM (For Reflash) 0 = external Flash
ED[1] [4]	I/O	Must be pulled high.
ED[3:2] [4]	I/O	Read on power-up to determine boot clock: Boot Clock ED[3] ED[2] CLKACQ 0 0 CLKACQ 1 1
ED[6:4] [4]	I/O	External bus data bits 4 to 6.
ED[7] [4]	I/O	Must be pulled low.
ED[15:8] [1, 4]	O	Upper 8 bits of the bi-directional system data but.
MWE, MOE [3]	O	External memory write enable and output enable.
SCLK	O	Test point.
SRESET	In	Input to FSM. The system reset that triggers an internally generated reset called RESET. The RTC counters are not affected by SRESET. Should be used only upon initial power-up of the device. Not for use to enter or exit hibernate mode.
Debug Interface Pins		
JTDI, JTCK, JTRST, JTMS	In	JTAG Interface. During boot-strap these pins determine RF reference frequency as follows: Frequency JTCK JTDI 16.369 MHz 0 0 24.5535 MHz 0 1 26.0 MHz 1 0 Reserved* 1 1 Strapping options cannot be used when in debug mode, software must configure ref freq setting. *Can also be programmed for 13, 16.8, or 19.2 MHz. See SiRF representative for details.
JTDO	O	Part of JTAG interface.
GPIO Lines [6]		
GPIO[0] [2, 4]	I/O	GPIO LNA Enable
GPIO[1] [2, 4]	I/O	GPIO Line. Alternate function is Odometer interface for SiRFDRive.
GPIO[2] [2]	I/O	GPIO Line. Alternate function is AGCPWM.
GPIO[4]	I/O	GPIO Line.Default state is input mode. Pad has no pull-up or pull-down resistor.
GPIO[9] [2,4]	I/O	GPIO Line (ALT = Timemark)
GPIO[10] [4]	I/O	GPIO Line. Alternate function is EIT[0]. Pad has no pull-up or pull-down resistor.

Table 2. GSC3e(f)/LPx Signal Description *(Continued)*

Signals	Type	Description
GPIO[13] 4	I/O	GPIO Line.Used for SiRFLoc aided GPS. Alternate function is CS1 or CTS.
GPIO[14] [1, 4]	I/O	GPIO Line. Alternate function is CS2 or RTS.
GPIO[15] [1, 4]	I/O	GPIO Line. Alternate function is CS3 or YCLK.
GSC3e(f)/LPx RF Signals		
CLKACQ_O	O	CLKACQ output.
GND_RF	Ground	
GRFRST	In	RF reset input signal from FSM.
RFIN	In	RFA input; GPS RF signal input. Must be AC coupled.
RTC_XI	In	RTC crystal oscillator input; a crystal network may be placed between this output and the RTC_XO input in lieu of using an external RTC oscillator.
RTC_XO	O	RTC crystal oscillator output; a crystal network may be placed between this output and the RTC_XI input in lieu of using an external RTC oscillator.
RTC_OUT	O	RTC crystal oscillator buffered output.
SPI_CEB, SPI_DI, SPI_CLK	In	RF synchronous serial interface (enable, data, and clock). Reserved for RF to digital interface.
SPI_DO	O	RF SPI interface output.
SIGN_MAG_O	O	SIGN and MAG combined output.
TP_IF	O	IF test point.
VCC_RF	Supply	RF supply; must be properly bypassed.
VCC_RTC	Supply	RTC oscillator supply; must be properly bypassed.
XTAL_IN	In	Reference oscillator input.
XTAL_OUT	Output	Reference clock output.
Peripheral Interface		
CTS [1, 5]	I/O	Clear to send/not, hardware flow control. Alternate function is GPIO[13].
EIT[0][4]	I/O	External interrupt[0]. Alternate function is GPIO[10].
ON_OFF	In	Edge triggered soft on or off request input to FSM. Message MID205 or ON_OFF pulse must be used to enter hibernate mode. ON_OFF pulse must be used to wake up from hibernate mode.
PLL_FILTER	Ana	External filter for PLL (analog pin).
RTS / CS[2] [1, 5]	I/O	Request to send/not, hardware flow control. Alternate functions are CS2 and GPIO[14].
RXA, RXB[1,6]	In	CMOS-level serial receive ports for channel A and B.
SI, SO, SK[2,4,5]	I/O	Digital synchronous serial interface (in, out and clock). Reserved for RF interface.
SS[0] [1, 5]	I/O	SPI slave select 0.
TIMEMARK[2,4,5]	I/O	Reserved. Alternate function GPIO[9].
TMODE	In	Reserved, tie Low.
TXA, TXB	O	CMOS-level serial message output ports for channel A and B.
YCLK[1,4,5]	In	Alt. functions: CS3 and GPIO[15].

Table 2. GSC3e(f)/LPx Signal Description *(Continued)*

Signals	Type	Description
RF Interface Pins		
CLKACQ_I	In	Data acquisition clock.
$\overline{\text{RESET}}$	OD	An FSM-generated RF chip reset based on $\overline{\text{SRESET}}$. This reset acts on the digital core, RF section, and any external devices controlled by $\overline{\text{RESET}}$.
RFPWRUP[3, 5]	O	Power control for RF chip LDO.
SIGN_MAG_I	In	Sign and magnitude bits.
RTC Interface Pins		
RIN	In	32 kHz clock input from RF section.
ROUT	O	No connect. May be used as a test point.
$\overline{\text{WAKEUP}}$	OD	Wake-up power control for baseband LDO from FSM (Open Drain). 3.6 V max.
All Supplies		
GND_BB (7)	Ground	GSC3e(f)/LPx digital GND.
VDD_BB (6)	Supply	Digital section and I/O supply.
VDD_FLASH	Supply	Flash power at 3 V (On GSC3f/LPx only).
VDDK	Supply	Core power at 1.2 V (if using VDD_REG, VDDK requires output bypass capacitor).
VDDPLL_O	Supply	Regulator output supply to PLL.
VDD_PLL_IN	Supply	Input power for PLL.
VDD_REG_IN	Supply	Power input to core regulator (3 V).
VDD_RTC	Supply	RTC/BBRAM/FSM circuit supply (1.2V).

Notes

1. Internal pull-up resistor (30kΩ nominal).
2. Internal pull-down resistor (30kΩ nominal).
3. Default output high at reset.
4. Default input at reset.
5. Share function with GPIO Line.
6. GPIO Lines are 3.3 V tolerant.
7. All GND and VCC pins must be connected to ensure reliable operation. Good RF design practices must be adhered to in the PC board layout. A ground plane and a power plane must be used to obtain good performance.

ELECTRICAL AND POWER SECTION

Electrical Specifications

This data sheet contains information about SiRF products in their development and sampling phases. SiRF reserves the right to make changes in its products, specifications and other information at any time without notice. SiRF assumes no liability or responsibility for any claims or damages arising out of the use of this data sheet, or from the use of integrated circuits based on this data sheet, including, but not limited to claims or damages based on infringement of patents, copyrights or other intellectual property rights. SiRF makes no warranties, either express or implied with respect to the information and specifications contained in this data sheet. Performance characteristics listed in this data sheet do not constitute a warranty or guarantee of product performance. All terms and conditions of sale are governed by the SiRF Terms and Conditions of Sale, a copy of which you may obtain from your authorized SiRF sales representative.

Table 3. Absolute Maximum Ratings

Parameter	Symbol	Rating	Units
Digital Core and I/O (Volatile)			
Power Supply Voltage	VDD_BB	3.15	V
Input Pin Voltage	VIN	5.25	V
Output Pin Voltage	VOUT	5.25	V
Latch-up Current (includes internal flash die)	ILATCH	±200	mA
Storage Temperature	TSTG	-65 to 150	°C
Battery Block (Non-Volatile) (RTC/BBRAM/FSM)			
Power Supply Voltage	VCC_RTC and VDD_RTC	2.0	V
Input Pin Voltage	VRIN	2.0	V
Output Voltage	VROUT	2.0	V
Open Drain Pull-Up Voltage	VOD	3.8	V
RF Section			
Maximum Supply Voltage	VCC_RF	3.15	V
Maximum DC Input (RFA)		10	dBm
Minimum DC Voltage on Any Pin	GND	-0.5	V
Maximum DC Voltage on Any Pin		3.15	V
RTC Voltage*	VCC_RTC	1.5	V

Note: Maximum recommended differential between VDD_BB and VCC_RF is 0.3 V.

* All RTC IO/FSM are 3.3 V tolerant, except for OSC pad, which is 1.65 V tolerant.

Table 4. Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Units
Power Supply Voltage	VDD_(all)	2.7	2.85	3.0	V
Power Supply Voltage	VCC_(all)	2.7	2.85	3.0	V
RTC/BBRAM/FSM Supply Voltage	VCC_RTC and VDD_RTC	1.1	1.2	1.3	V
Operating Temperature	TOPR	-40		85	°C
Peak Acquisition Current [1] + Internal Flash	IDD		26 2.8		mA
Avg Acquisition Current [2] + Internal Flash	IDD		23 1.3		mA
Tracking Current [3] + Internal Flash	IDD		22 1.0		mA
Standby Current [4]	IDD		1.5		mA
External Reference Amplitude (when driven externally, XTALIN must be ac-coupled)		200	-	1200	mVpp
Ext. Ref. Frequency Range		13	-	26	MHz
RF front end gain		14		26	dB

Notes

1. Peak acquisition current is characterized by millisecond bursts above average acquisition current.
2. Avg acq. current is typically only the first two seconds of TTFF.
3. Tracking current typically includes tracking and the post-acquisition portion of TTFF.
4. During standby state: RTC block and core remain powered on but clock is off.
5. RTC must always be powered during chip operation.

Table 5. Battery Conditions

Parameter	Symbol	Min.	Typ.	Max.	Units
RTC Supply	VCC_RTC and VDD_RTC	1.1	1.2	1.3	V
Supply Current [1, 2]	IDDRTC		10		µA
Power Supply[2]	VDD	0	0	0	V

Notes

1. GSC3e(f)/LPx includes a HIBERNATE state from which it can restart itself.
2. All external I/O lines must be driven low or disabled during battery back-up or HIBERNATE state.

Warning – Stressing the device beyond the “Absolute Maximum Ratings” may cause permanent damage. These are stress ratings only. Operation beyond the “Operating Conditions” is not recommended and extended exposure beyond the “Operating Conditions” may affect device reliability.

DC CHARACTERISTICS

Table 6. DC Electrical Characteristics for RTC Block (Non-Volatile Digital Section)

(Pins: RIN, ROUT, $\overline{\text{WAKEUP}}$, ON_OFF, $\overline{\text{SRESET}}$, $\overline{\text{RESET}}$, and TMODE)

Parameter	Symbol	Min.	Typ.	Max.	Conditions	Units
High Level Input Voltage	V_{IH}	0.7 *V_{DDRTC}		V_{DDRTC} +0.3		V
Low Level Input Voltage	V_{IL}	-0.3		0.3*V_{DDRTC}		V
Switching Threshold	V_T		0.5*V_{DDRTC}			V
High Level Input Current	I_{IH}	-10		10 60	V_{IN} = V_{DD} with pull-down	µA
Low Level Input Current	I_{IL}	-10		10 -60	V_{IN} = V_{SS} with pull-up	µA
High Level Output Voltage	V_{OH}	V_{DDRTC} -0.2			I_{OH} = 100 µA	V
Low Level Output Voltage	V_{OL}			0.2	I_{OL} = 100 µA	V
Input Capacitance	C_{IN}			5	Input or Bi-directional	pF
Output Capacitance	C_{OUT}			5	Output Buffer	pF
Output Current	I_{OH} and I_{OL}			2	None	mA
Output Current (Rout only)	I_{OH} and I_{OL}			1	None	mA

Table 7. DC Electrical Characteristics (Volatile Digital Section)

Parameter	Symbol	Min.	Typ.	Max.	Conditions	Units
High Level Input Voltage	V_{IH}	0.7*V_{DD}		V_{DD}+0.3		V
Low Level Input Voltage	V_{IL}	-0.3		0.3*V_{DD}		V
Switching Threshold	V_T		0.5*V_{DD}			V
High Level Input Current	I_{IH}	-10		10 60	V_{IN} = V_{DD} with pull-down	µA
Low Level Input Current	I_{IL}	-10		10 -60	V_{IN} = V_{SS} with pull-up	µA
High Level Output Voltage	V_{OH}	*V_{DD} -0.2			I_{OH} =100 µA	V
Low Level Output Voltage	V_{OL}			0.2	I_{OL} = 100 µA	V
Tri-State Output Leakage	I_{OZ}	-10		10	V_{OUT} = V_{SS} or V_{DD}	µA
Input Capacitance	C_{IN}			5	Input or Bi-directional	pF
Output Capacitance	C_{OUT}			5	Output Buffer	pF
Output Current (Memory bus)	I_{OH} and I_{OL}			4	None	mA
Output Current (GPIO and others)	I_{OH} and I_{OL}			2	None	mA

Table 8. GSC3e(f)/LPx DC Electrical Characteristics (RF Section)

All specifications under conditions T=25°C, VCC=2.85 V.

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Total Supply Current SPI Mode Sleep (RF domain) Normal Power Clock Only Mode	I_{CC}	 - - -	 0.006 13 1	 0.009 15	mA	 Full Power Acq Clk and RTC only
SPI CMOS Input High Level	V_{ih}	VCC_RF * 0.8	-	-	V	
SPI CMOS Input Low Level	V_{il}	-	-	VCC_RF * 0.2	V	

AC CHARACTERISTICS (GSC3e/LPx)

All measurements in Table 9 and Table 10 are characterized except as noted with (*) which are guaranteed by design.

Table 9. AC Characteristics for Write Access

Parameter List	Timing	Min.[2]	Max.[2]	Unit
$\overline{CS} \longrightarrow \overline{MWE}$	T1	5.6	9	ns
EA $\longrightarrow \overline{MWE}$	T2	10	12	
$\overline{MWE}$ Pulse Width [1]	T3	59.1	60	
$\overline{MWE} \longrightarrow \overline{CS}$	T4	11.7	18.1	
$\overline{MWE} \longrightarrow$ EA	T5	29.5	30.4	

1. With two wait states; width = 20.13 + (#WS x 20*)

* CPU clock periods

2. Min and Max values are from best and worst operating conditions

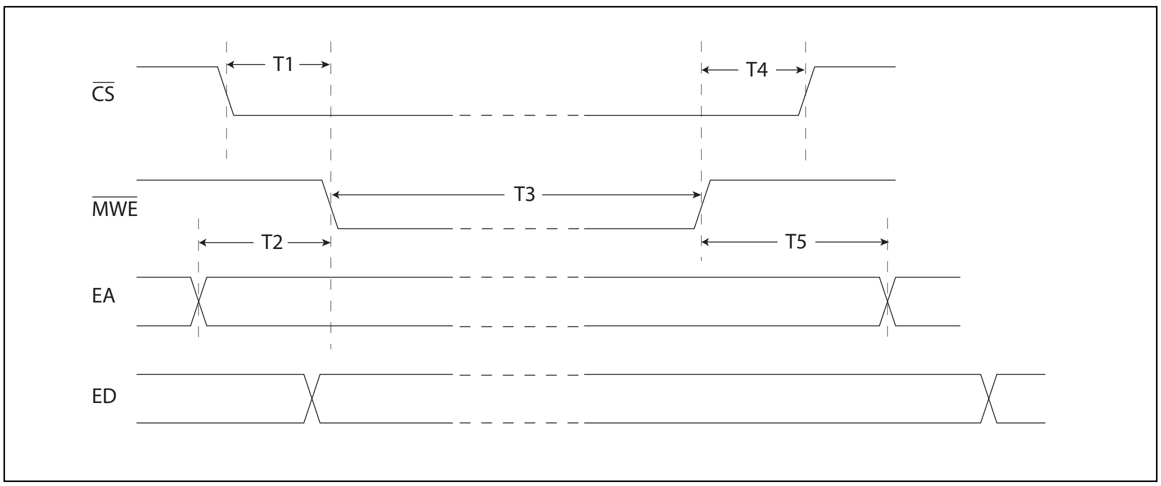


Figure 6. Write Access Timing Diagram

Table 10. AC Characteristics for Read Access (GSC3e/LPx)

Parameter List	Timing	Min.[2]	Max.[2]	Unit
$\overline{CS}$ → $\overline{MOE}$	T1	5.9	8.9	ns
EA → $\overline{MOE}$	T2	10.1	11.4	
ED → $\overline{MOE}$	T3	15.4	18	
$\overline{MOE}$ Pulse Width [1]	T4	60	60.6	
$\overline{MOE}$ → $\overline{CS}$	T5	11.5	17	
$\overline{MOE}$ → EA	T6	48.7	50.1	

1. With two wait states; width = 20.13 + (#WS x 20*)
* CPU clock periods
2. Min and Max values are from best and worst operating conditions

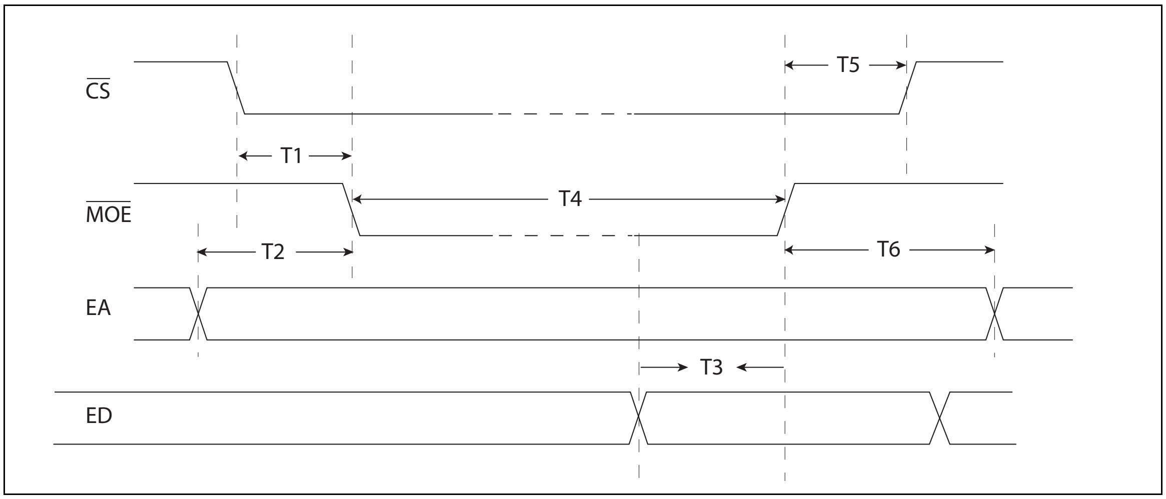


Figure 7. Read Access Timing Diagram

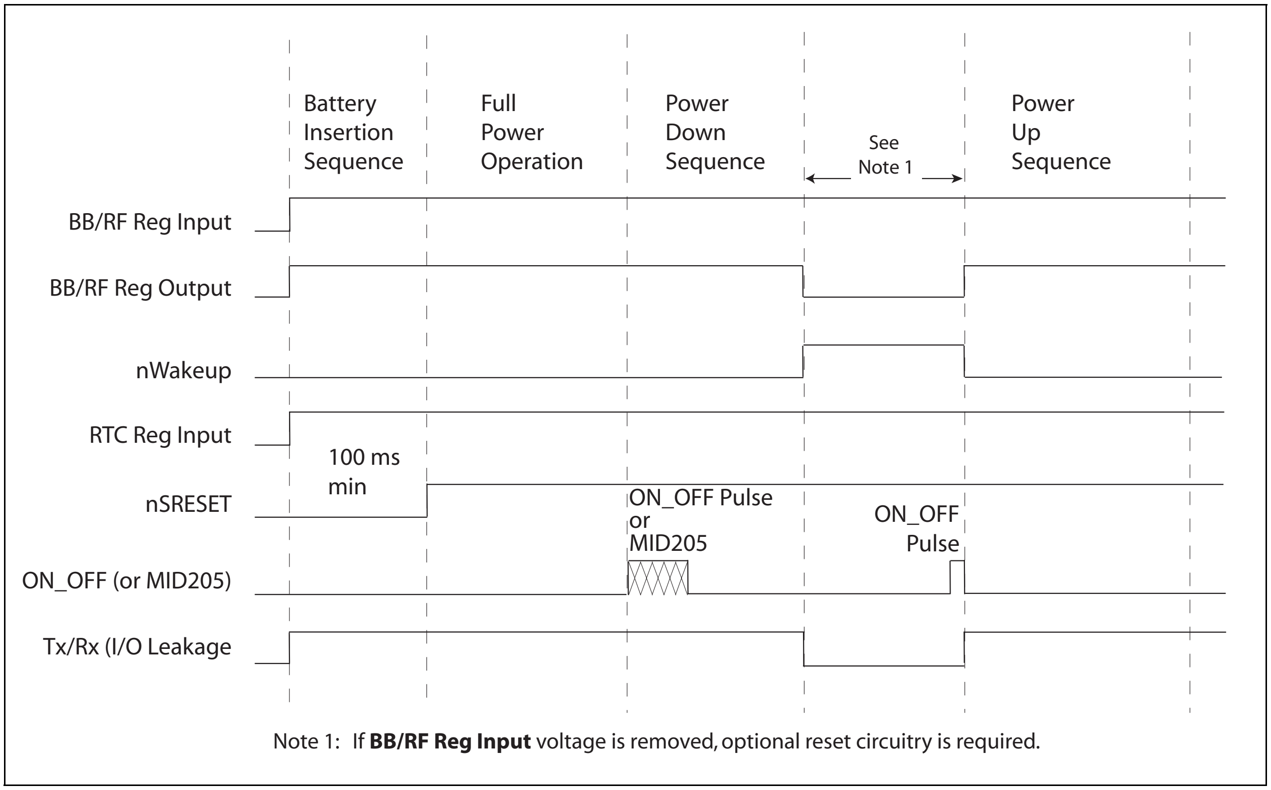


Figure 8. Power Sequencing Diagram

Table 11. GSC3e(f)/LPx Thermal Characteristics

Parameter	Symbol	Typical	Units	Conditions
Thermal Resistance Junction-to-Ambient	θ_{dJA}	40	°C/W	

Table 12. GSC3e(f)/LPx RF Section AC Characteristics

All specifications under conditions T=25°C, VCC=2.85 V.

All RF measurements are made with appropriate matching to the input or output impedance.

AC Characteristic	Symbol	Min.	Typical	Max.	Units	Conditions
RFA/Mixer/AGC						
Noise Figure (AGC @ min. Gain)	NF	-	6.0	11	dB	
Input 1 dB Gain Compression (AGC @ min. Gain)	IP_{1db}	-	-65	-	dBm	
Input Return Loss w/ External Match (Fig 10)	RL	-	9.5	-	dB	
Image Rejection Ratio (AGC @ min. Gain)		20	-	-	dB	
IF Filter/AGC-AMP						
Filter Attenuation at 12 MHz	F(12 MHz)	20	-	-	dB	
Filter Bandwidth	BW	-	7	-	MHz	3 dB bandwidth
Voltage Gain Resolution		-	1.7	-	dB	
Gain Adjust Range		45	51	-	dB	
Minimum Receiver Gain		-	50	-	dB	
Maximum Receiver Gain		-	100	-	dB	
Gain Linearity		-2.0	-	2.0	dB	
Frequency Synthesizer						
Operating Frequency			1571.424		MHz	
Type of Synthesizer		Integer-N				
Reference Frequency		13	-	26	MHz	6 discrete frequencies
Reference Input Level		200	-	1200	mVpp	50% duty (1)
CMOS Driver						
Logic Level High	V_{oh}	$V_{CC\_IO\_EXT}$ * 0.9	-	-	V	
Logic Level Low	V_{ol}	-	-	$V_{CC\_IO\_EXT}$ * 0.1	V	
Rise Time @ 12 pF Load (10% to 90%)		-	4.0		ns	
Fall Time @ 12 pF Load (90% to 10%)		-	4.0		ns	
Static Sink Current and Source Current		VCC ÷ 5 kΩ	-	-	mA	

(1) Must meet performance standards defined in SiRF TCXO SSIII performance specification.

Table 13. Operating Modes

Operating Modes	Comments
Normal Power	Entire chip enabled (normal operation).
CPU ONLY	The RF section PLL and receiver chain are disabled. All other circuits are powered. This mode is used during low power operations such as TricklePower or Advanced Power Management. It allows the GSC3e(f)/LPx to save power by shutting down portions of the RF section while it is idle and the SiRFstarIII core and ARM are still performing.
STANDBY	The RF section is disabled. The digital section clocks are idle. The RTC and battery back up sections are powered. This mode allows the GSC3e(f)/LPx to minimize power consumption while the chip is in brief idle period such as during a power management cycle.
HIBERNATE	All circuits except the RTC from ON_OFF and battery-backed SRAM are disabled. Can wake-up at a preset time or by external interrupt Vin from ON_OFF.

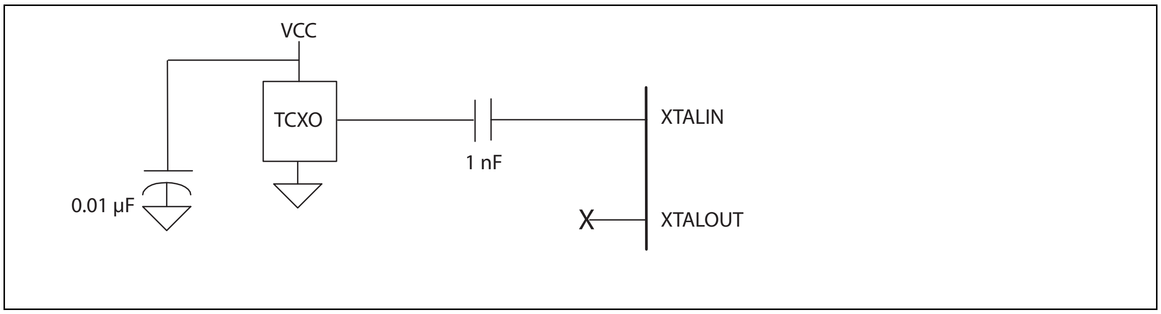


Figure 9. Typical TCXO Circuitry

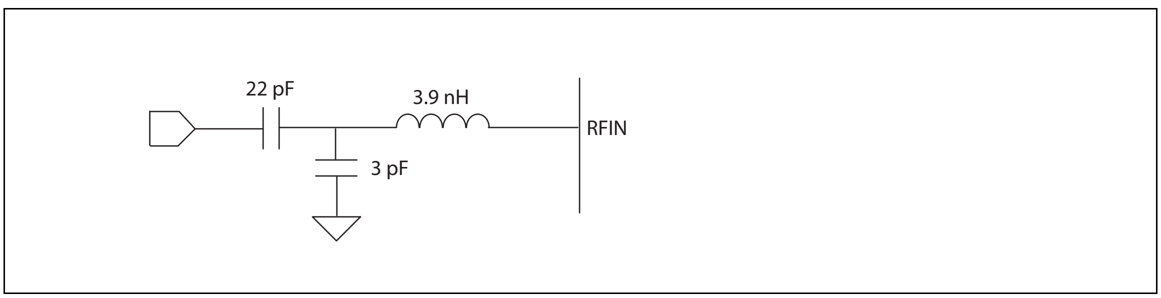


Figure 10. Sample RFIN Input Impedance Matching Circuitry

INPUT IMPEDANCE SMITH CHARTS

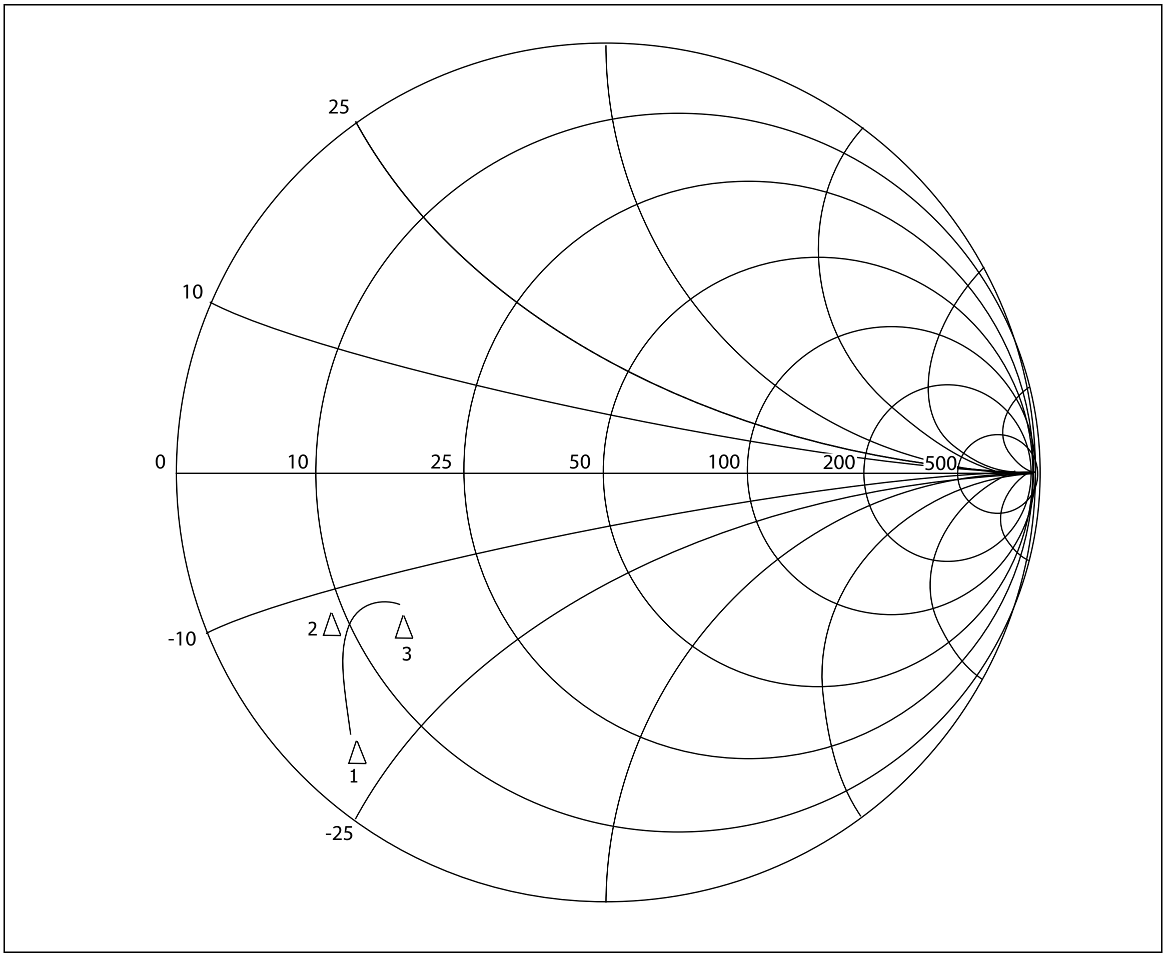


Figure 11. Narrowband Input Impedance Smith Chart for GSC3e(f)/LPx

Table 14. RFA Input Impedance Over Frequency (S11)

Test Conditions: RF Input = -60 dBm, Zo = 50Ω, 2.85 V, 25°C. No matching circuitry was used for these measurements.

Marker	1	2	3
Frequency	1,475 MHz	1,575 MHz	1,675 MHz
Impedance	6.7 - j 20.6 Ω	9.9 - j 15.4 Ω	16.4 - j 15.0 Ω

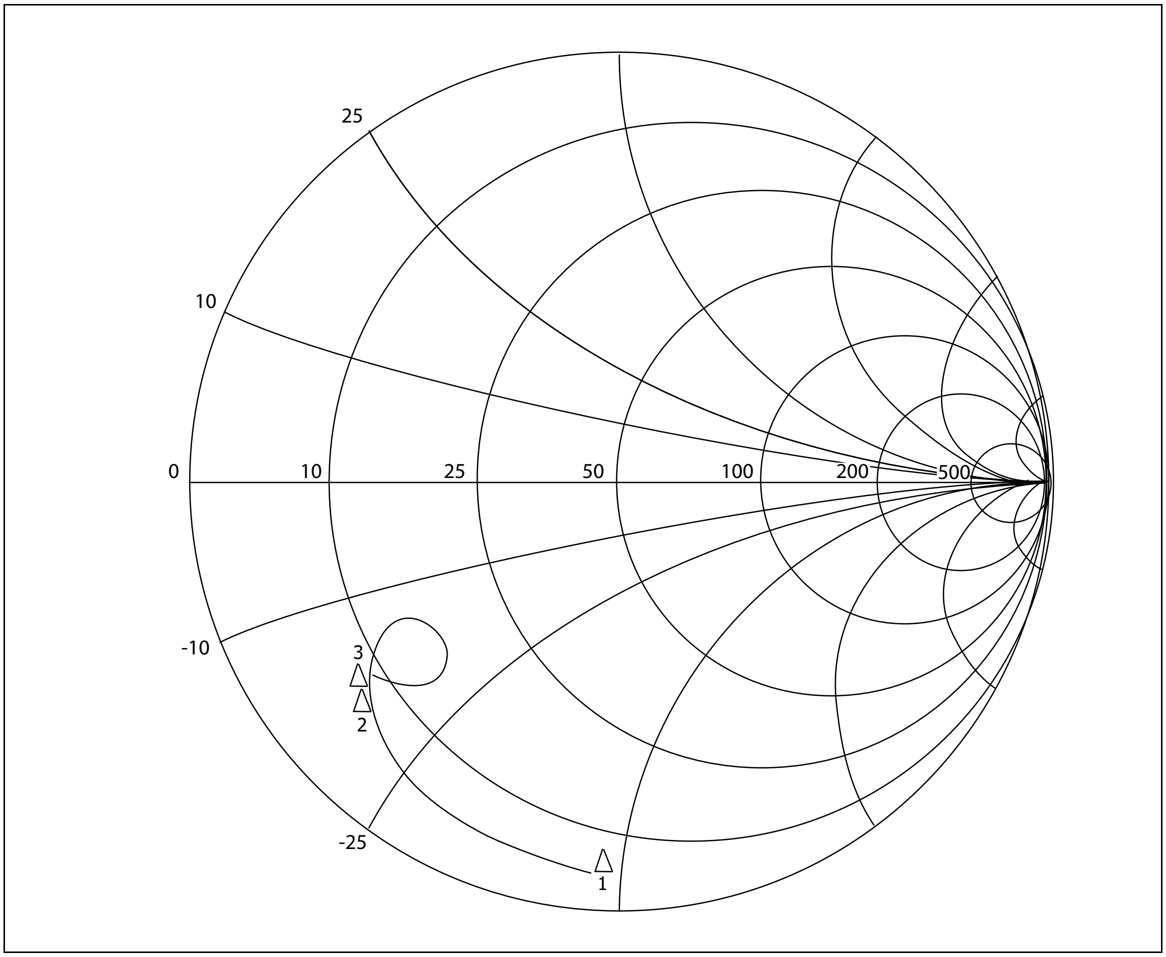


Figure 12. Wideband Input Impedance Smith Chart for GSC3e(f)/LPx

Table 15. RFA Input Impedance Over Frequency (S11)

Test Conditions: RF Input = -60 dBm, Zo = 50Ω, 2.85 V, 25°C. No matching circuitry was used for these measurements.

Marker	1	2	3
Frequency	1,000 MHz	1,575 MHz	2,000 MHz
Impedance	5.489 - j 44.76 Ω	9.572- j 15.38 Ω	8.66- j 15.36 Ω

MECHANICAL SECTION

Mechanical Specifications- Packaging Diagram

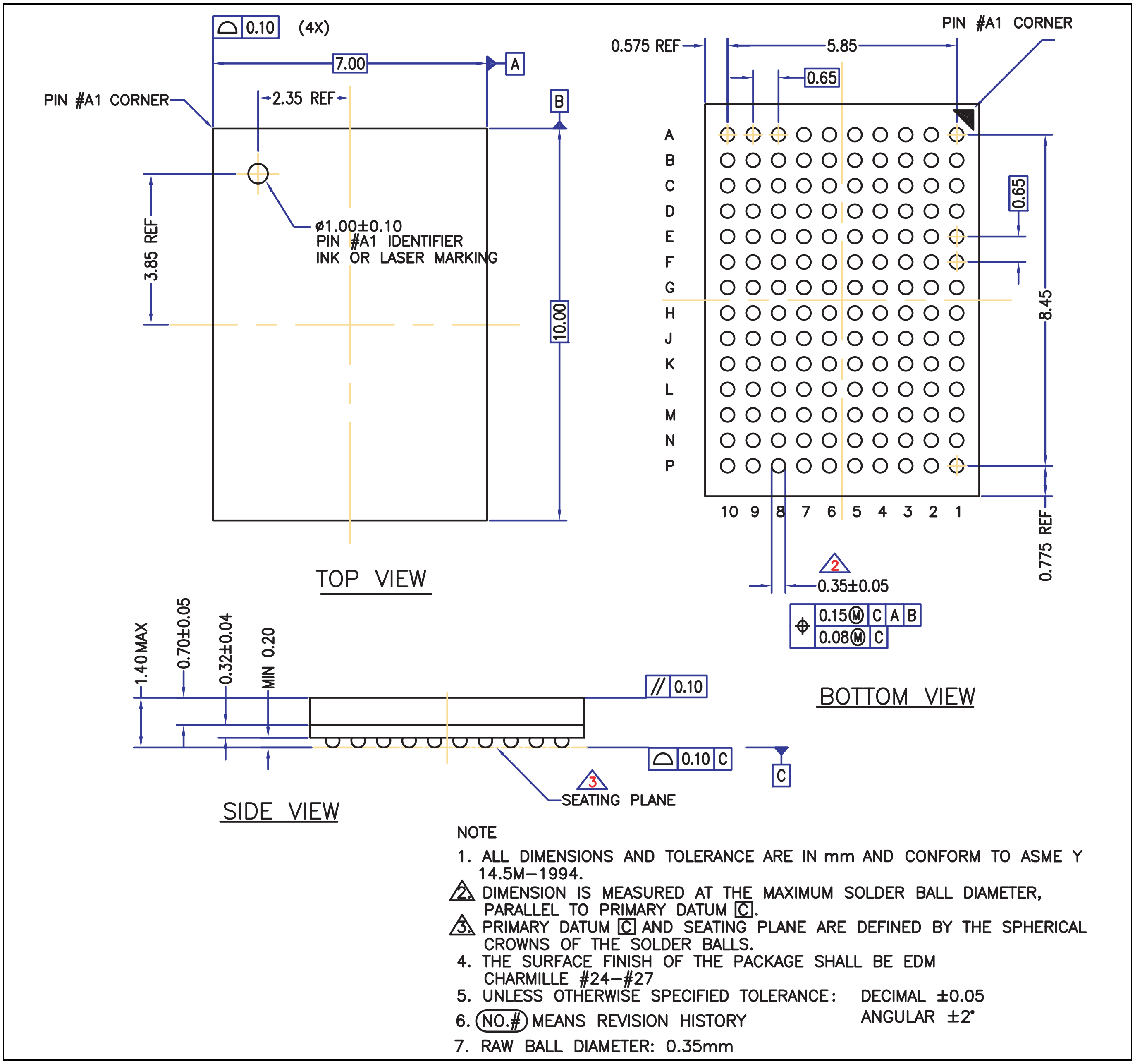


Figure 13. GSC3e(f)/LPx 140 PIN BGA Package

Additional Information

SiRF has Evaluation Kits available for this product to allow you to conduct various performance tests. SiRF also supports developers through the availability of a system Developer Kit which includes access to application notes and reference designs; and support from SiRF engineers for design, testing, troubleshooting, and prototype evaluation. SiRF GSW firmware may also be modified through a SiRF firmware developer kit which allows limited modification and configuration of SiRF standard firmware, as well as incorporation of a small amount of user code. Additional ARM development tools must be purchased separately.

Ordering Information

Part Number	Description
GSC3e/LPx-7985	GSC3e/LPx, 16-bit, 140-pin, BGA, Lead-Free
GSC3f/LPx-7989	GSC3f/LPx, 16-bit, 140-pin, BGA, Lead-Free
Development Tools	
9900-0286	GSC3e(f)/LPx Evaluation Kit
9900-0293	GSC3e(f)/LPx System Development Kit (SDK)

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